Electronic Version
Stylesheet Version v1.1.1

GATE CONTROLLED FLOATING WELL VERTICAL MOSFET

Abstract

A novel transistor structure for a DRAM cell includes two deep trenches, one trench including a vertical storage cell for storing the data and the second trench including a vertical control cell for controlling the p-well voltage, which, in effect, places part of the p-well in a floating condition thus decreasing the threshold voltage as compared to when the vertical pass transistor is in an off-state. This enables the transistor to exhibit increased gate overdrive and drive current during an active wordline voltage commonly applied to both gates of the storage and control cells.